Why 1D for electronics applications

PURDUE UNIVERSITY Discovery Park Birck Nanotechnology Center

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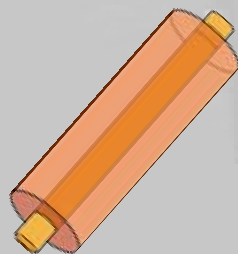
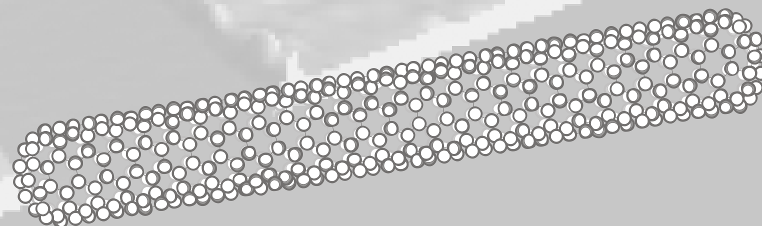
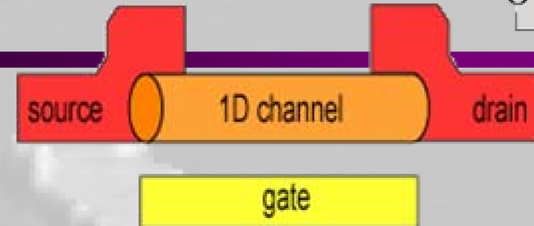




MRSEC meeting, October 17

Advantages of 1D - electrostatics



The chain of arguments:

"Nano" allows for improved electrostatics

Improved electrostatics allows to reduce the device length

$$\lambda = \sqrt{t_{ox} t_{body} \frac{\varepsilon_{body}}{\varepsilon_{ox}}}$$

A reduced device length …

1) … increases the device speed

2) … allows for higher device density

3) … reduces the power consumption

Advantages of 1D – band movement

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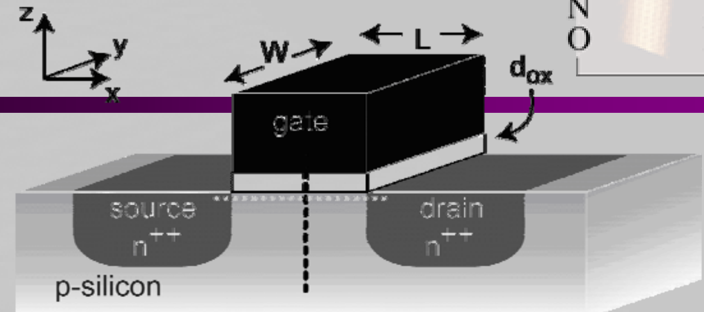
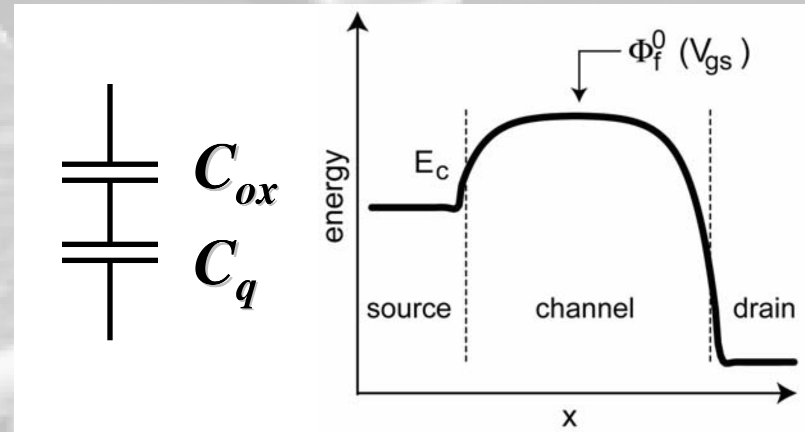


… but there is more …

$$C_{\rm tot} = e\frac{\partial Q_{\rm tot}}{\partial \Phi_{\rm g}} = \frac{C_{\rm ox}C_{\rm q}}{C_{\rm ox}+C_{\rm q}}$$

$$C_{\rm q} = e\frac{\partial Q_{\rm tot}}{\partial \Phi_{\rm f}^0}$$

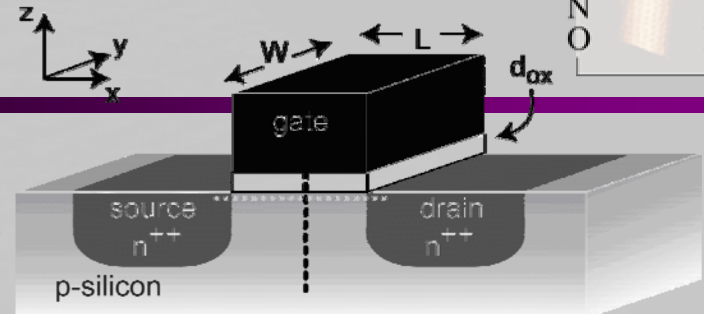


$$\delta\Phi_{\rm f}^0 = \frac{C_{\rm ox}}{C_{\rm ox}+C_{\rm q}}\delta\Phi_{\rm g}$$

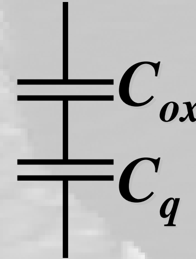
$$\begin{cases} C_{ox} << C_q \quad : \quad \delta\Phi_f^0 \to 0 \\ C_q << C_{ox} \quad : \quad \delta\Phi_f^0 \approx \delta\Phi_g \end{cases}$$

$$C_{\rm q}^{\rm 1D} \approx e^2\, L\, T_{\rm SB}(E_{\rm f}^{\rm s} - \Phi_{\rm f}^0)D^{\rm 1D}(E_{\rm f}^{\rm s} - \Phi_{\rm f}^0)$$

Advantages of 1D – quantum capacitance



… but there is more …



$$C_{tot} = e\frac{\partial Q_{tot}}{\partial \Phi_g} = \frac{C_{ox}C_q}{C_{ox}+C_q}$$

$$C_{ox} \sim \frac{L}{t_{ox}}$$

classical limit

$$C_{tot} \approx C_{ox}$$

$$\tau = \frac{C_{tot}V_{dd}}{I_d} \sim L^2$$

$$P \cdot \tau = C_{tot}V^2 \sim \frac{L}{t_{ox}}$$

diffusive: $I_d \sim \frac{C_{tot}}{L^2}$

$$C_q \sim L$$

quantum capacitance limit

$$C_{tot} \approx C_q$$

$$\tau = \frac{C_{tot}V_{dd}}{I_d} \sim L^2$$

$$P \cdot \tau = C_{tot}V^2 \sim L$$

Advantages of 1D - quantum capacitance

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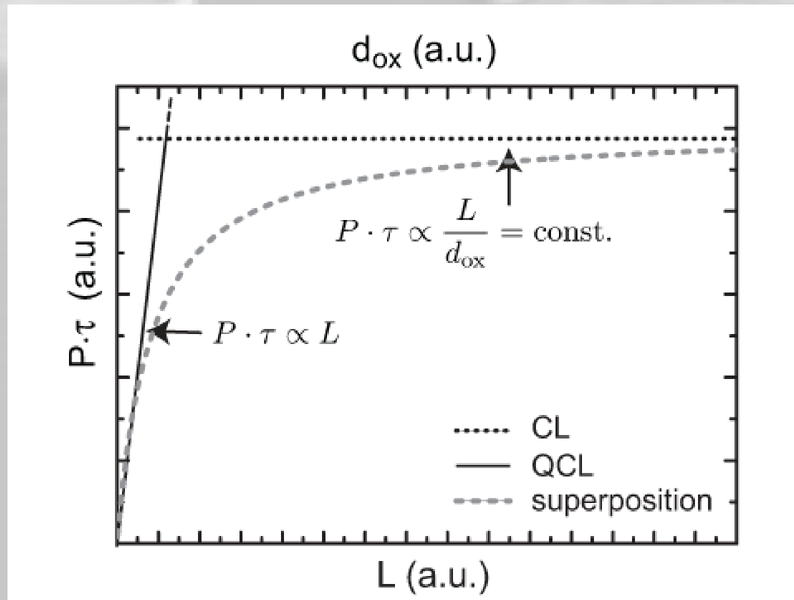
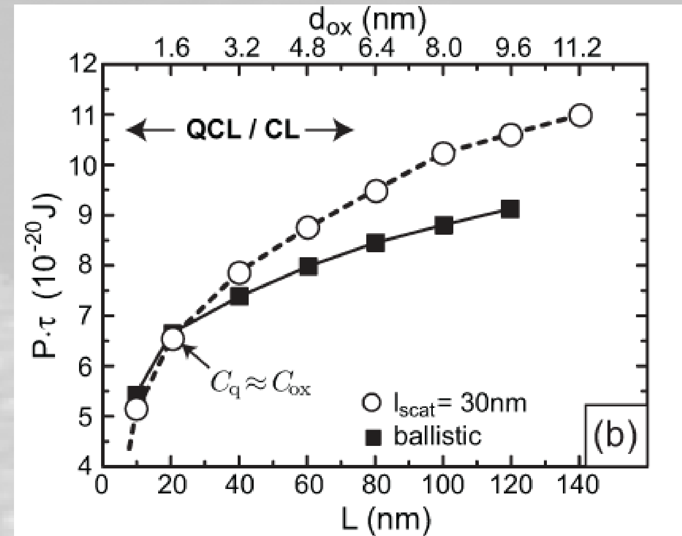
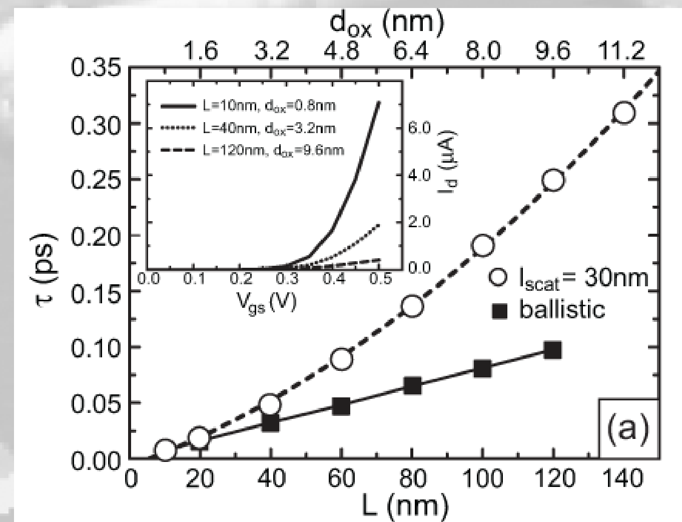
… but there is more …



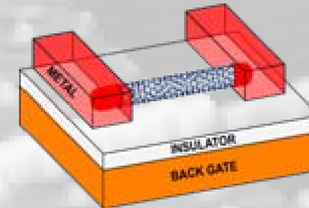




IEEE Electron Device Letter **29**, 372 (2008)

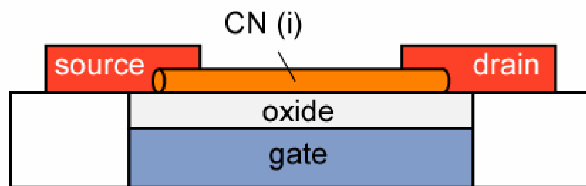
Device considerations for CNFETs

What is the right choice of CNFET layout?

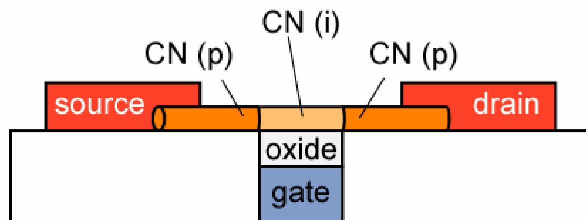


Electrical characteristics for various CNFET layouts?

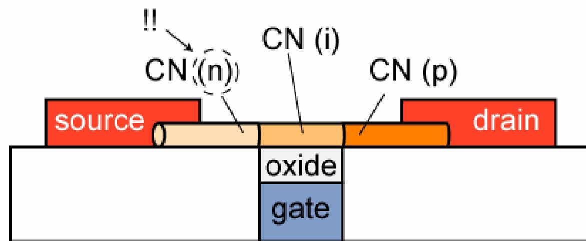
a) SB-CNFET

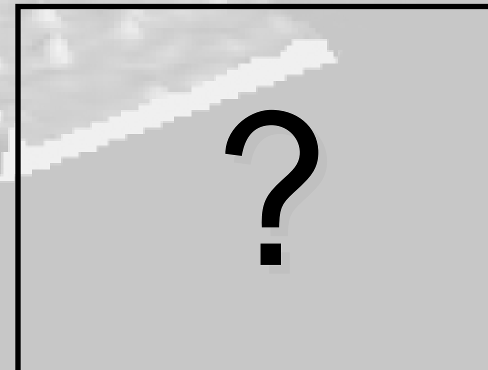


b) C-CNFET (p-type)

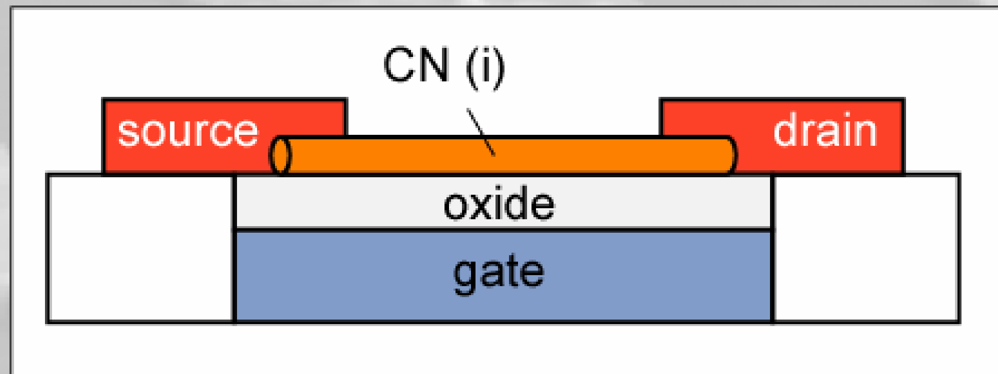


c) T-CNFET (p-type)

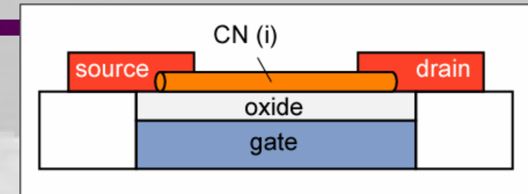




The SB-CNFET



The SB-CNFET



simulation results

V_{ds} = 0.1V, t_{ox} = 5nm

Φ_B

source

drain

V_{gs}: -0.5V to +0.9V

steps: 0.2V

potential [eV]

channel length [nm]

I_d [A]

V_{gs} [V]

V_{ds} = 0.1V

V_{ds} = 0.3V

V_{ds} = 0.5V

L = 30nm, t_{ox} = 5nm, Φ_B = 0.3eV

transfer1

- electron and hole injection is possible

Phys. Rev. Lett. **89**, 126801 (2002), Appl. Phys. Lett. **83**, 2435 (2003)

The SB-CNFET

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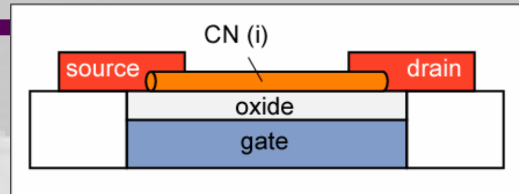
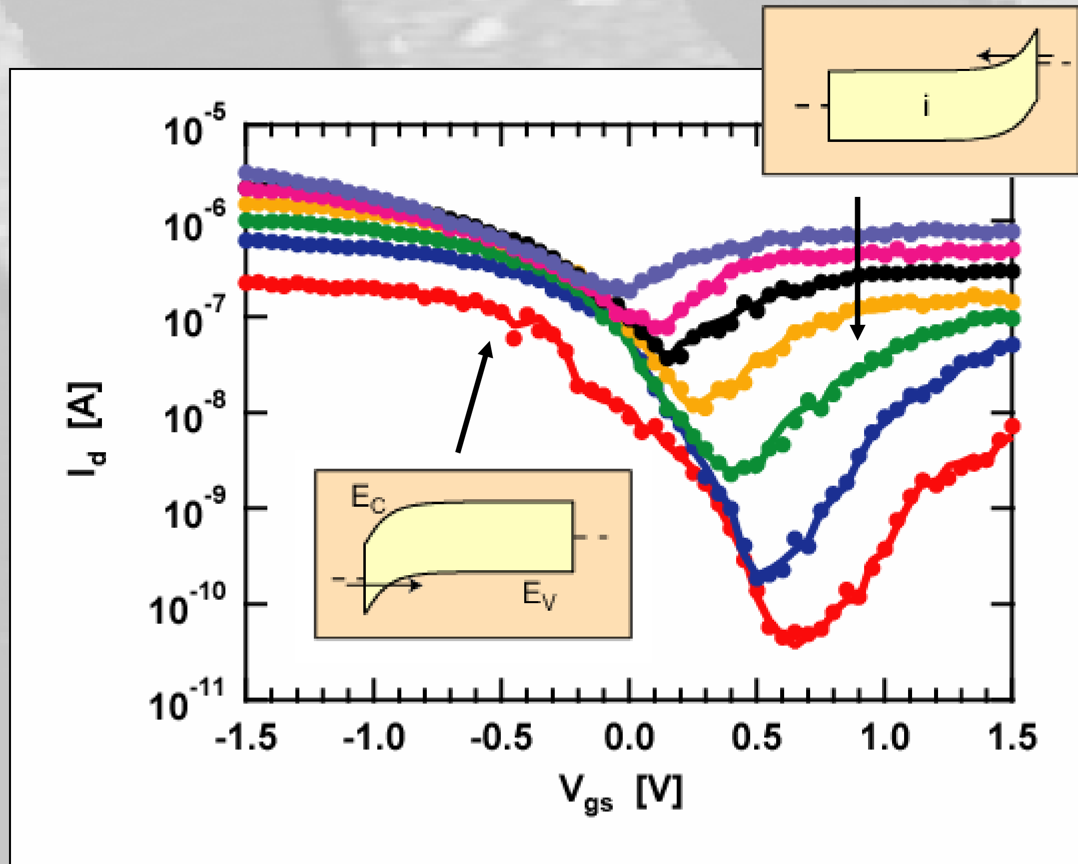


experimental results



L = 300nm

t_{ox} = 10nm

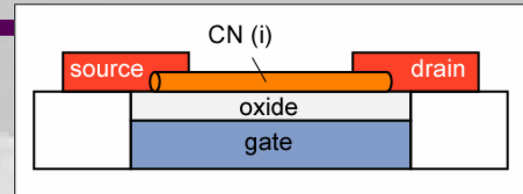
t_{NT} = 1.8nm

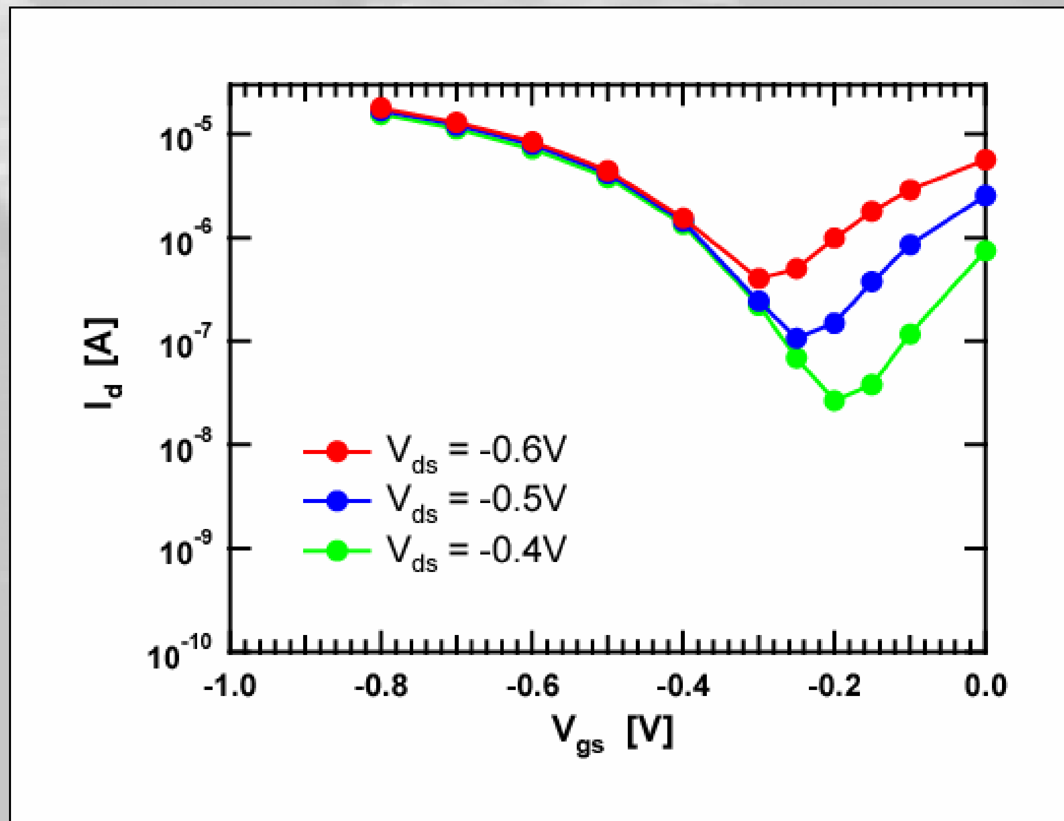
Ti - contacts

planar gated

The SB-CNFET

simulation results





L = 20nm

t_{ox} = 1nm

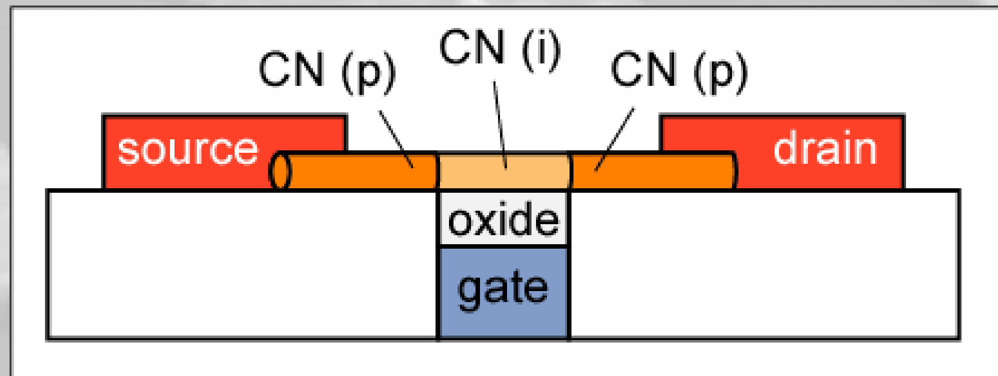
t_{NT} = 1.8nm

Pd - contacts

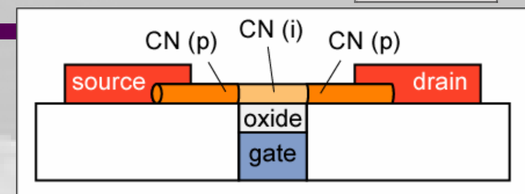
wrap around

Appl. Phys. Lett. **83**, 2435 (2003)

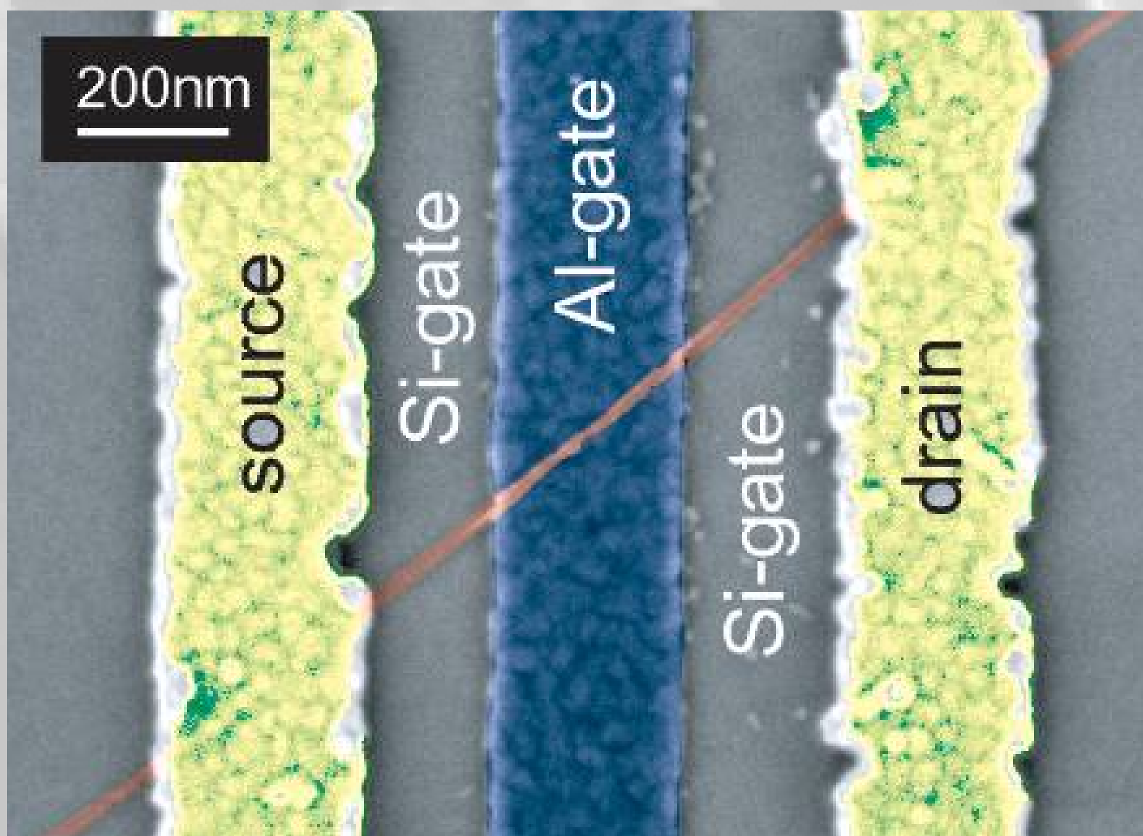
The C-CNFET



The C-CNFET

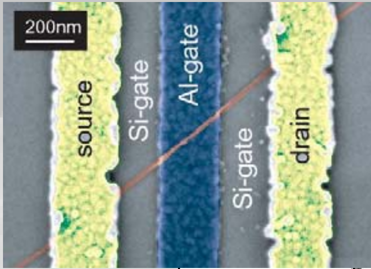


experimental results

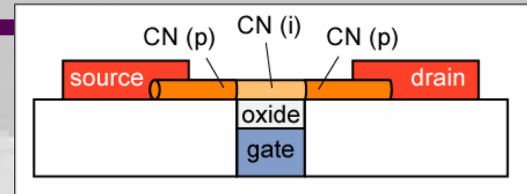


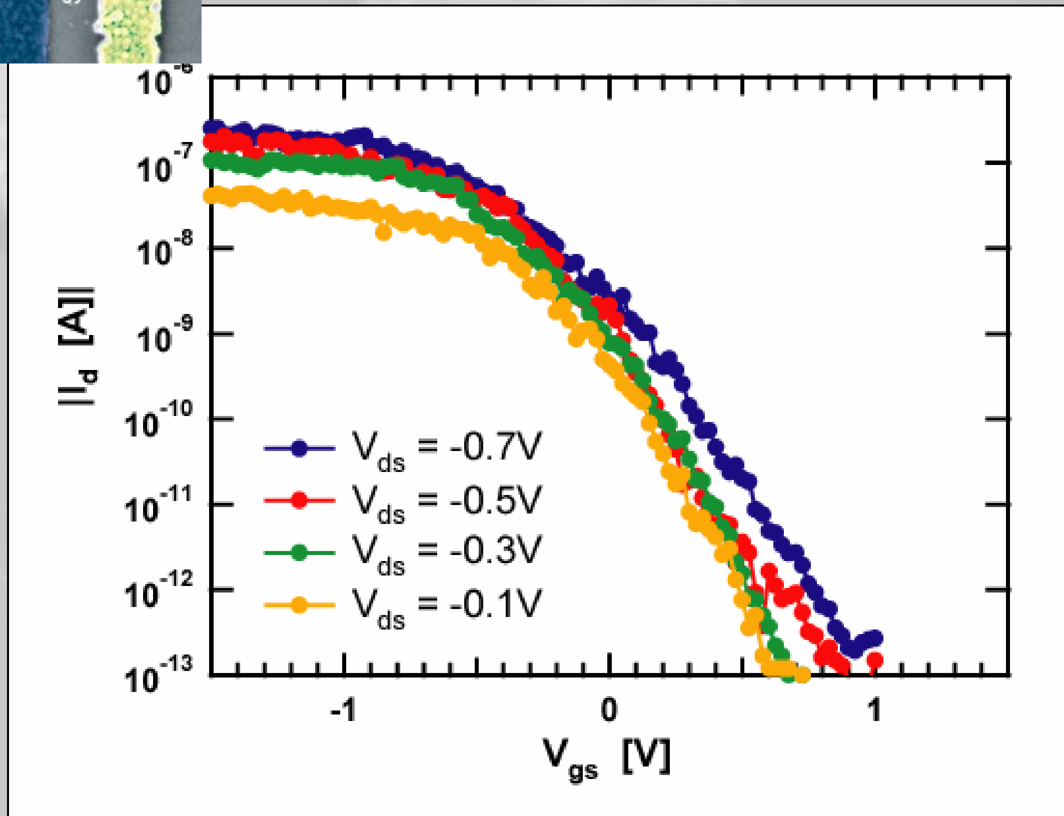
Phys. Rev. Lett. **93**, 196805 (2004)

The C-CNFET



experimental results





L = 200nm

t_{ox} = 4nm

t_{NT} = 1.8nm

Ti - contacts

planar gated

IEEE Transactions on Nanotechnology **4**, 481 (2005)

The C-CNFET

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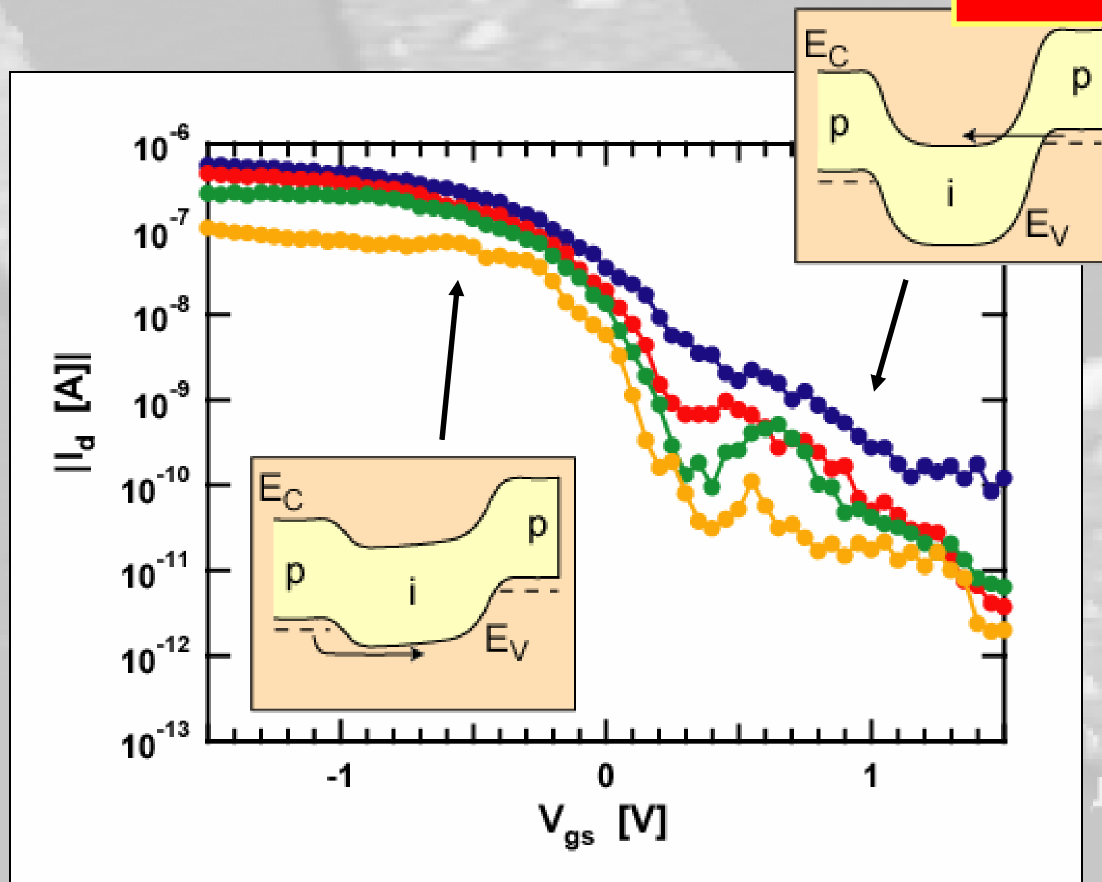
CN (p) CN (i) CN (p)

source drain oxide

charge pile-up

experimental results



$L = 40\text{nm}$

$t_{ox} = 4\text{nm}$

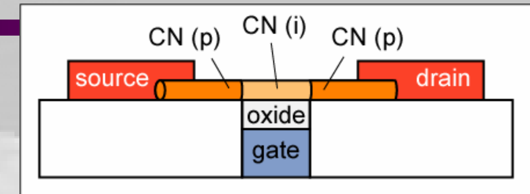
$t_{NT} = 1.8\text{nm}$

Pd - contacts

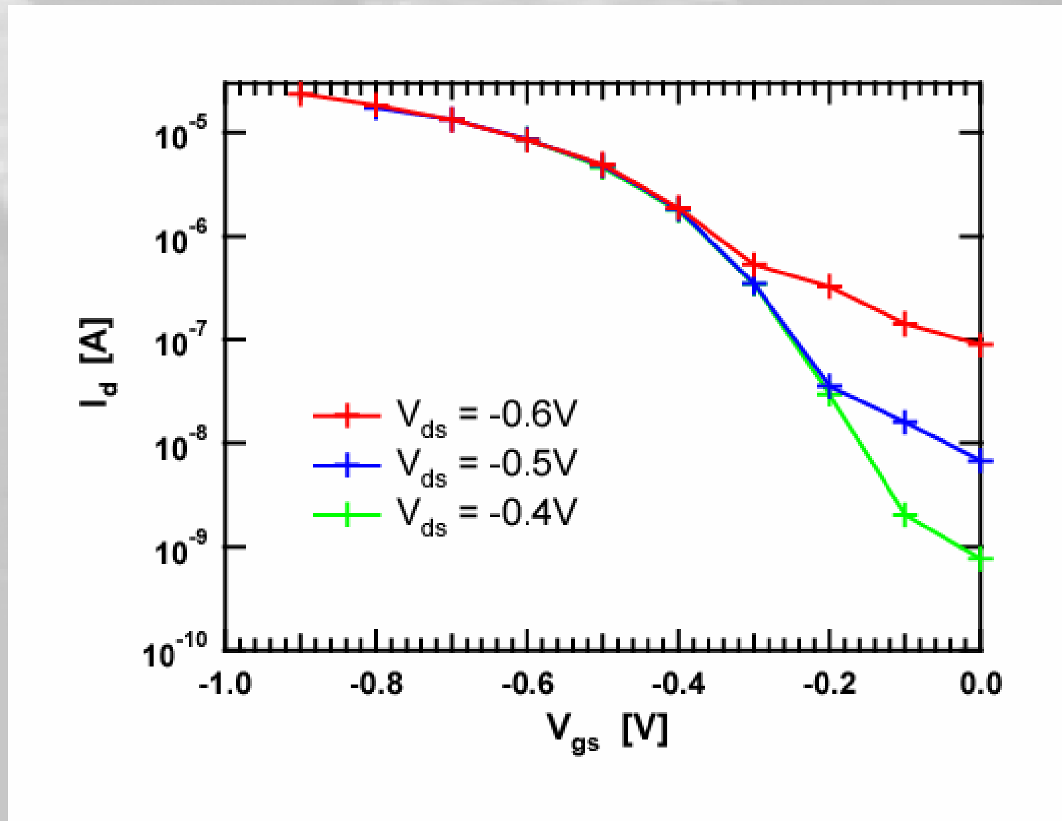
planar gated

IEEE Transactions on Electron Devices **52**, 2568 (2005)

The C-CNFET



simulation results



L = 20nm

t_{ox} = 1nm

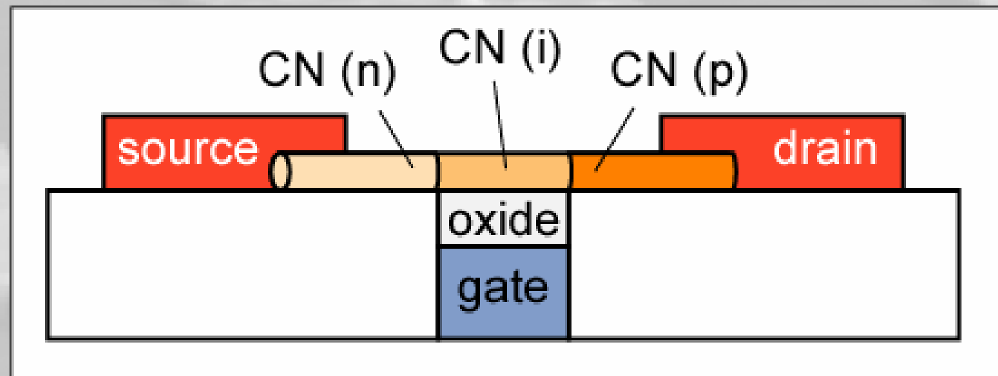
t_{NT} = 1.8nm

Pd - contacts

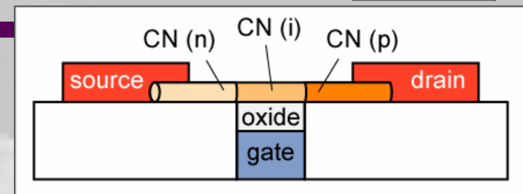
wrap around

Solid State Electronics **49**, 73 (2005)

The T-CNFET

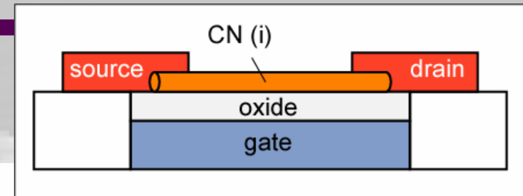


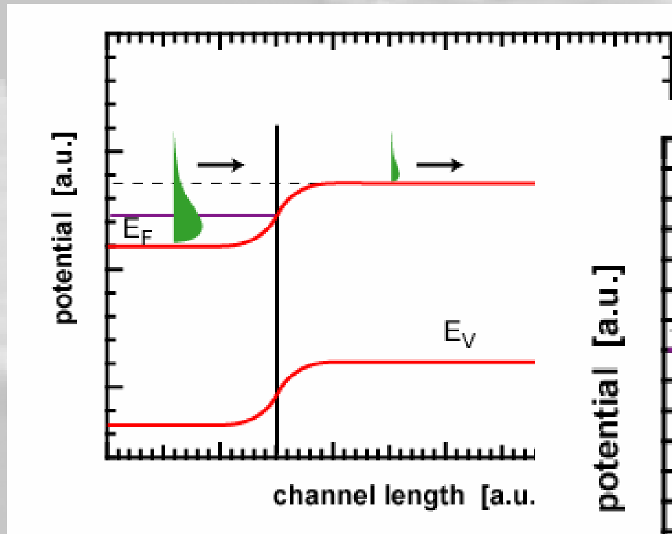
The T-CNFET

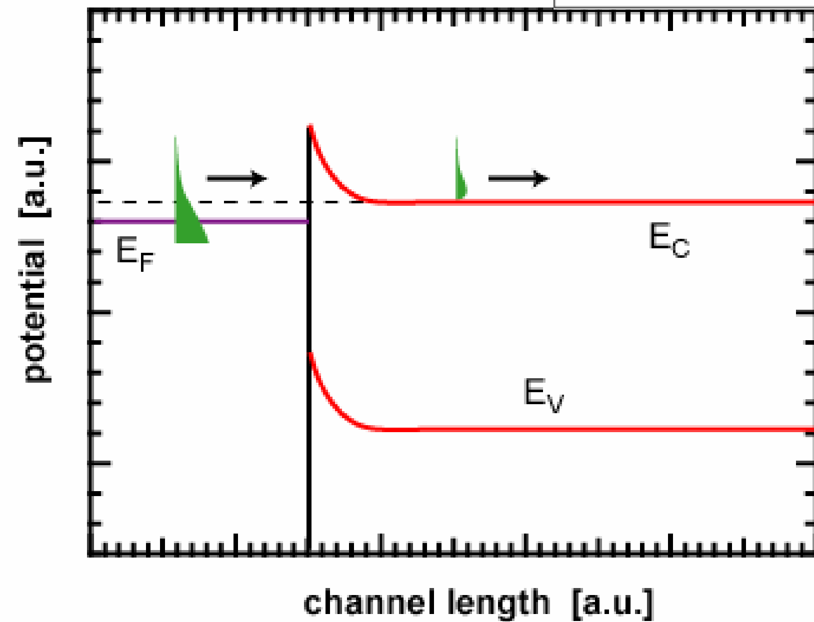


IEEE Transactions on Electron Devices **52**, 2568 (2005)

The T-CNFET and the SB-CNFET



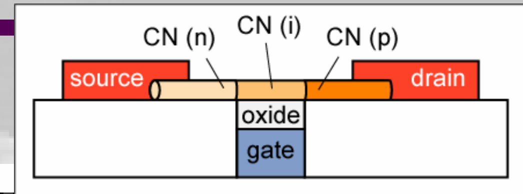


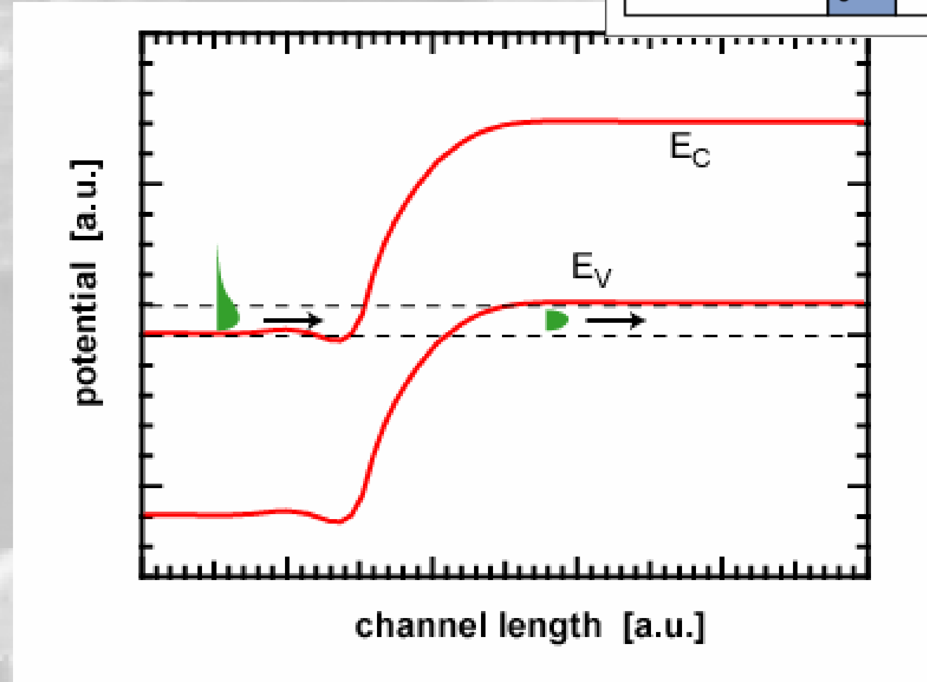


$$S_{\min} = \frac{k_B T}{|e|} \ln(10)$$

The inverse subthreshold slope S is always larger than ~60mV/dec at room-temperature for a conventional MOSFET and even more so for an SB-CNFET

The T-CNFET

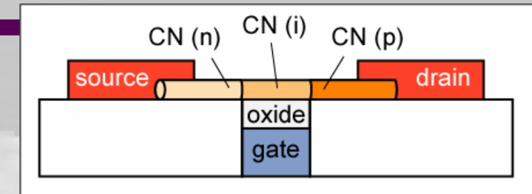




$$S_{\min} \sim \not{k_B T}$$

A filter-like arrangement can potentially make S smaller than 60mV/dec

The T-CNFET



- The semiconductor is one-dimensional
- The body of the semiconductor is ultra-thin
- Transport in the semiconductor is ballistic
- The effective masses of electrons and holes are small
- The effective masses of electrons and holes are similar
- The semiconductor has a direct band gap

The T-CNFET

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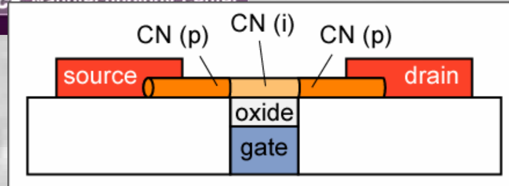
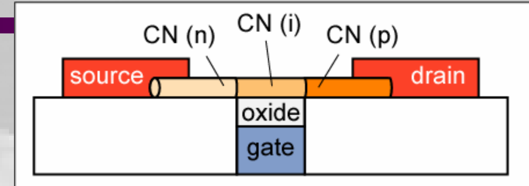
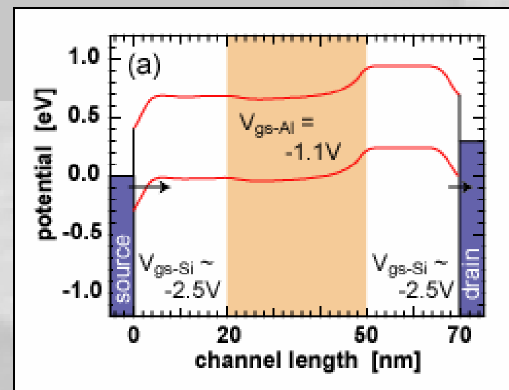
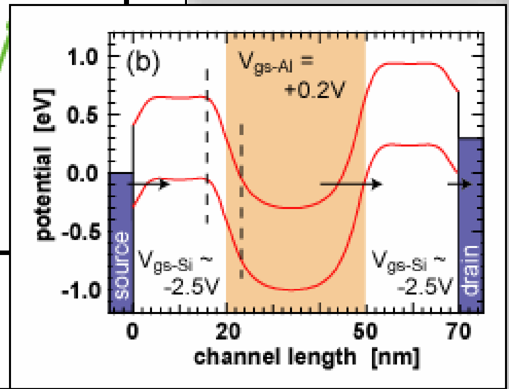




experimental results

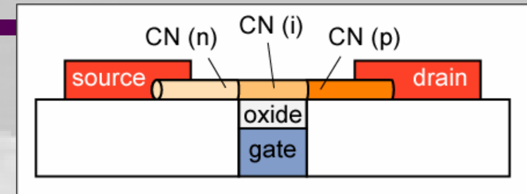


(a)
measurement at T = 300K
I_d [A]
10^{-9}
10^{-10}
10^{-11}
10^{-12}
10^{-13}
10^{-14}
10^{-15}
S ~ 65 $\frac{mV}{dec}$
S ~ 40 $\frac{mV}{dec}$
(b)
simulation
t_{ox-Al} = 2.5nm
t_{ox-Al} = 5nm
t_{ox-Al} = 10nm
-1.5
-1.0
-0.5
0.0
V_{gs-Al} [V]

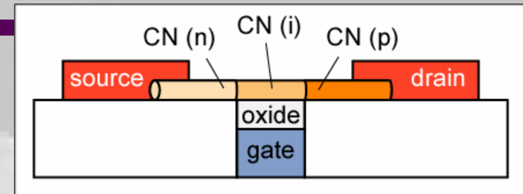


Phys. Rev. Lett. **93**, 196805 (2004)

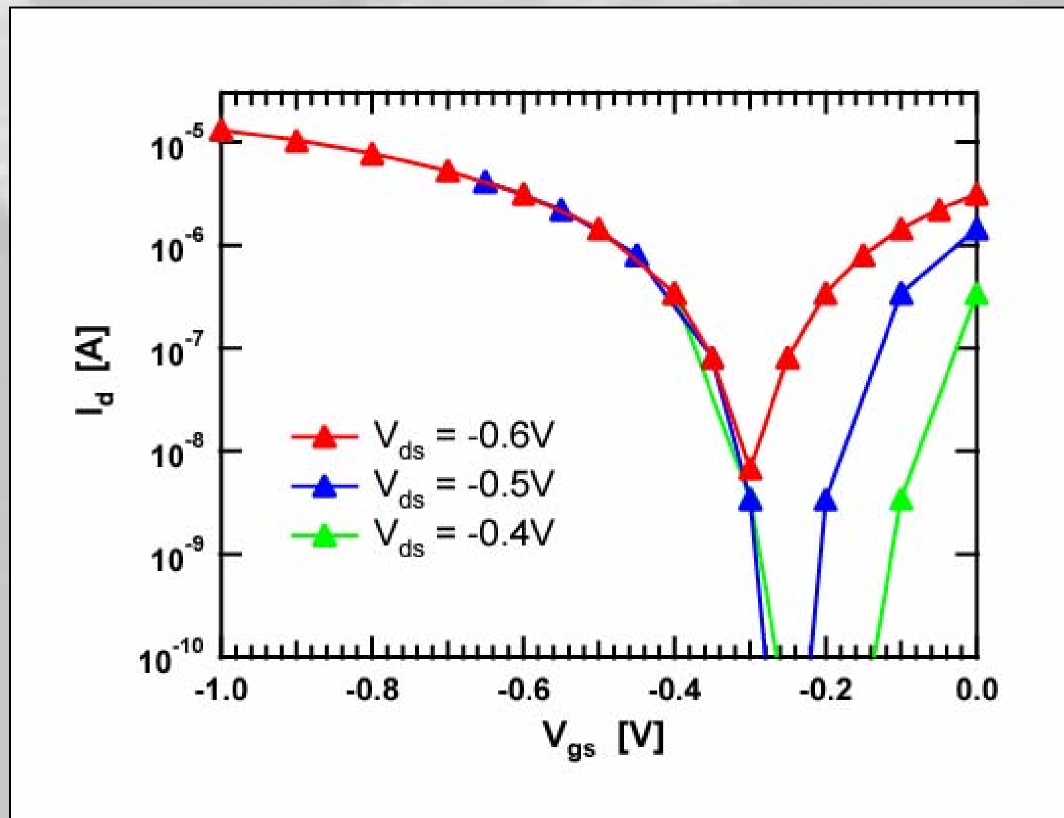
The T-CNFET



The T-CNFET



simulation results



L = 20nm

t_{ox} = 1nm

t_{NT} = 1.8nm

Pd - contacts

wrap around

IEEE Transactions on Electron Devices **52**, 2568 (2005)

Electrical characteristics for various CNFET layouts!

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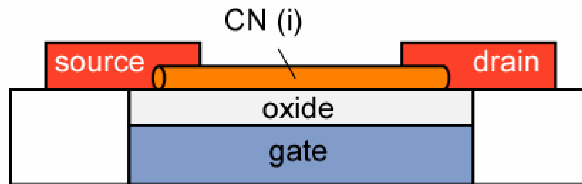
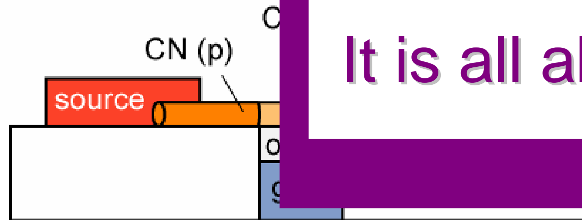
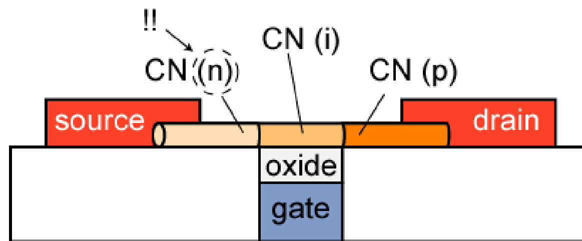
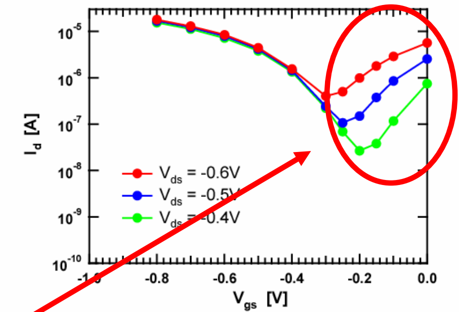
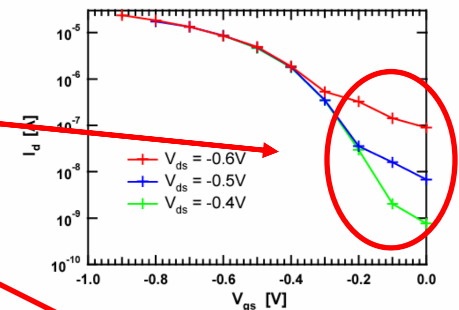
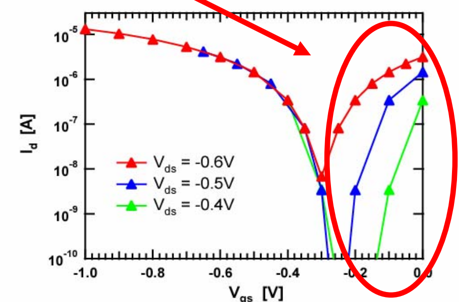








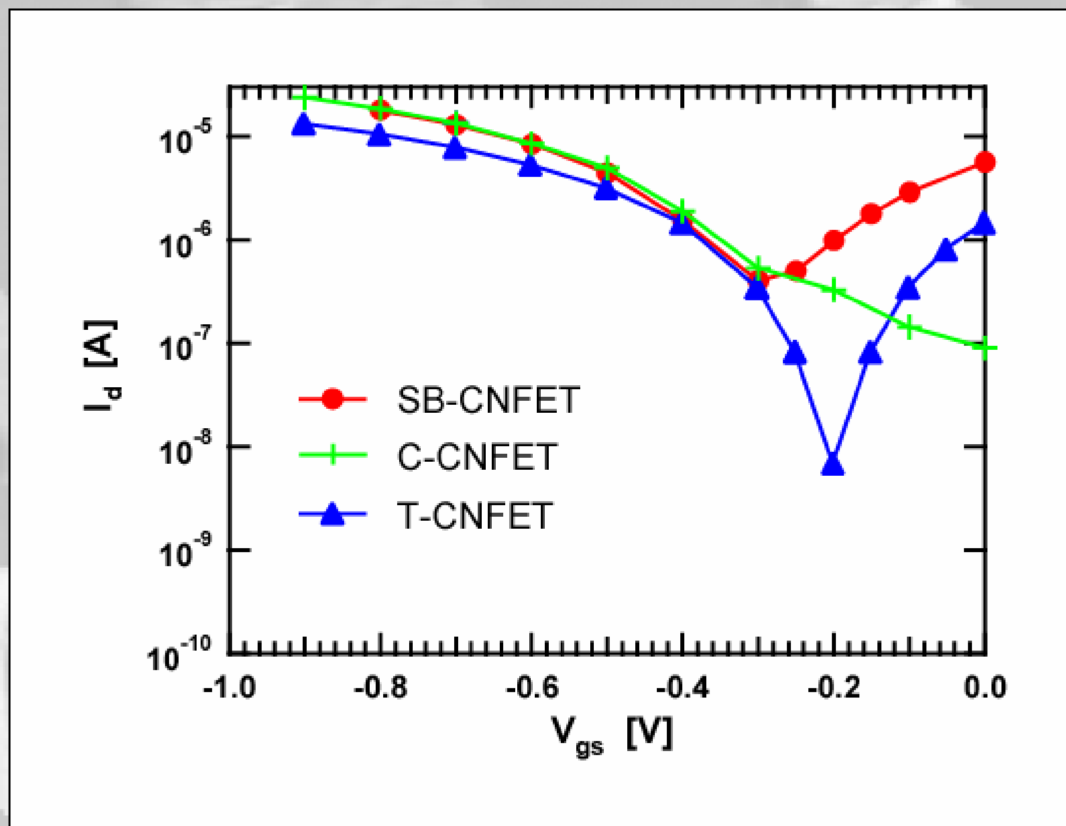




It is all about tunneling

Electrical characteristics for various CNFET layouts!

simulation results



The ideal choice: A novel tunneling device design

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